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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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KIM, H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/984,562	Mailloux et al,
Examiner	**Group Art Unit**
H. Kim	2185

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 5/4/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 22-32, 59, 60, 61 & 63-72 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 22-32 & 59-72 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____ ☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892 ☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Other_____

Office Action Summary

Detailed Action

1. Claims 22-32, 59-61, 63-65, and 66-72 are presented for examination. Claims 66-72 have been added by the amendment filed on 5/4/01. This office action is in response to the Amendment filed on 5/4/01.

2. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 22-32, 59-61, and 63-65 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 22, *Manning* discloses the invention as claimed. *Manning* discloses a memory circuit, comprises control logic (Fig. 1 Ref. 38 and col.6 lines 26-32); selection and temporary

storage circuit (Fig. 1 ref. 18); and a multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address or internal counter, col. 8 lines 58+) for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50).

As to claims 23 and 24, Manning. further discloses external mode select signal and enable signal (Fig. 1 Ref 38 and col.6 lines 26-32).

As to claim 25, Manning. further discloses write enable and output enable (Fig. 2).

As to claim 26, Manning. further discloses a counter (Fig. 1 Ref. 26).

As to claim 27, Manning. further discloses the counter is used in the burst mode (col. 4 lines 47-49 and col. 8 line 67).

As to claim 28, *Manning* further discloses a second external address (col. 6 lines 14+ and col. 5 lines 43-50).

As to claim 29, Manning. further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claims 30 and 31, Manning further discloses no CAS delay latency during a write cycle (col. 5 lines 66+) and at least a two CAS latency during read cycle (col. 7 lines 36-37).

As to claim 32, Manning further discloses an asynchronously accessible memory array (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 59, *Manning* discloses a memory circuit (Fig. 1), comprises control logic (Fig. 1 Ref. 38 and col.6 lines 26-32); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24); a multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address or internal counter, col. 8 lines 58+); and the control signal for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 42-50), wherein the memory circuit is an asynchronous dynamic random access memory circuit (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 60, *Manning* disclose the invention as claimed in claim 22. *Manning* further discloses control logic for providing an external address (col. 6 lines 14+) and the control logic for receiving the first external address and the external mode control signal respectively therefrom and for switching the memory circuit between a first mode of operation and a second mode of operation (col. 6 lines 14+).

As to claim 61, *Manning* disclose the invention as claimed in claim 22. *Manning* further discloses control logic for providing an internal mode control signal (Fig. 1, col. 7 lines 28+, control of /OE signal, CAS latency, and burst length read on this limitation, and col.6 lines 26-32).

As to claim 63, *Manning* disclose the invention as claimed. *Manning* discloses a memory circuit, comprises control logic for providing a selected mode control signal (Fig. 1 Ref. 38, col.6 lines 26-32 and col. 7 lines 28+); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24) and a second external address (col. 5 lines 43-50); a first multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19); a second multiplexer (Fig. 1 Ref. 26, selection of external address or internal counter, col. 8 lines 58+); and the control logic for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50).

As to claim 64, *Manning* further disclose a counter (col. 8 lines 58+).

As to claim 65, *Manning* disclose the invention as claimed. *Manning* discloses a memory circuit, comprises control logic for providing a mode control indicating a pipelined mode (col. 5 lines 43-50) or a burst mode of operation (col. 6 lines 14+); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24) and a second

external address (col. 5 lines 43-50); a counter (col. 8 lines 58+); and a pair of multiplexer (Fig. 1 Ref 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address or internal counter, col. 8 lines 58+).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 22-32, 59-61, 63-65, and 66-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burst DRAM Function & Pinout, Oki Electronic Ind. Co., Ltd (Oki), JC42.3, Albuquerque, 2nd presentation, item # 619, September 1994 in view of *Manning*, U.S. Patent 5,610,864.

As to claim 66, *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). Although Oki discloses control logic (page 2 BE pin) for burst and normal page, Oki does not specifically disclose selection and temporary storage circuit; and a multiplexer for switching the memory circuit between a burst and a pipelined mode of operation.

Manning discloses selection and temporary storage circuit (Fig. 1 ref. 18); and a multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and

selection of external address or internal counter, col. 8 lines 58+) for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50) because it would provided high speed data access and for compatibility with new and latest protocols and devices (abstract 2-3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate selection and temporary storage circuit and a multiplexer for switching the memory circuit between a burst and a pipelined mode of operation of Manning in the invention of Oki because it would provide high speed data access and for compatibility with new industry standard and latest protocols or devices thereby more marketable. The advantage of increasing the memory speed provide sufficient suggestion and motivation to one of ordinary skill in the memory art to follow the teaching of Manning into invention of Oki.

As to claims 67 and 68, Manning. further discloses external mode select signal and enable signal (Fig. 1 Ref 38 and col.6 lines 26-32).

As to claim 69, Manning. further discloses a write enable signal (Fig. 2 /WE).

As to claim 70, Manning. further discloses an output enable signal (Fig. 2 /OE).

As to claim 71, Manning. further discloses a counter (Fig. 1 Ref. 26).

As to claim 72, Manning. further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claim 22, *Oki* and Manning disclose the invention as claimed in claim 66. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). *Manning* further discloses a memory circuit, comprises control logic (Fig. 1 Ref. 38 and col.6 lines 26-32); selection and temporary storage circuit (Fig. 1 ref. 18); and a multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address or internal counter, col. 8 lines 58+) for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50).

As to claims 23 and 24, Manning. further discloses external mode select signal and enable signal (Fig. 1 Ref 38 and col.6 lines 26-32).

As to claim 25, Manning. further discloses write enable and output enable (Fig. 2).

As to claim 26, Manning. further discloses a counter (Fig. 1 Ref. 26).

As to claim 27, Manning. further discloses the counter is used in the burst mode (col. 4

lines 47-49 and col. 8 line 67).

As to claim 28, *Manning* further discloses a second external address (col. 6 lines 14+ and col. 5 lines 43-50).

As to claim 29, Manning. further discloses EDO modes (col. 4 line 50), pipeline mode (col. 5 lines 43-50), and burst mode (col. 7 lines 28+).

As to claims 30 and 31, Manning further discloses no CAS delay latency during a write cycle (col. 5 lines 66+) and at least a two CAS latency during read cycle (col. 7 lines 36-37).

As to claim 32, Manning further discloses an asynchronously accessible memory array (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 59, *Oki* and Manning disclose the invention as claimed in claim 66. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). *Manning* further discloses a memory circuit (Fig. 1), comprises control logic (Fig. 1 Ref. 38 and col.6 lines 26-32); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24); a multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address

or internal counter, col. 8 lines 58+); and the control signal for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 42-50), wherein the memory circuit is an asynchronous dynamic random access memory circuit (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16).

As to claim 60, *Oki* and Manning disclose the invention as claimed in claim 22. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). *Manning* further discloses control logic for providing an external address (col. 6 lines 14+) and the control logic for receiving the first external address and the external mode control signal respectively therefrom and for switching the memory circuit between a first mode of operation and a second mode of operation (col. 6 lines 14+).

As to claim 61, *Oki* and Manning disclose the invention as claimed in claim 22. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). *Manning* further discloses control logic for providing an internal mode control signal (Fig. 1, col. 7 lines 28+, control of /OE signal, CAS latency, and burst length read on this limitation, and col.6 lines 26-32).

As to claim 63, *Oki* and Manning disclose the invention as claimed in claim 22. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial

external address (page 2 A). *Manning* further discloses a memory circuit, comprises control logic for providing a selected mode control signal (Fig. 1 Ref. 38, col.6 lines 26-32 and col. 7 lines 28+); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24) and a second external address (col. 5 lines 43-50); a first multiplexer (Fig. 1 Ref. 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19); a second multiplexer (Fig. 1 Ref. 26, selection of external address or internal counter, col. 8 lines 58+); and the control logic for switching the memory circuit between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50).

As to claim 64, *Manning* further disclose a counter (col. 8 lines 58+).

As to claim 65, *Oki* and Manning disclose the invention as claimed in claim 22. *Oki* discloses a memory circuit, comprising: control logic (page 2 BE pin) and receiving an initial external address (page 2 A). *Manning* further discloses a memory circuit, comprises control logic for providing a mode control indicating a pipelined mode (col. 5 lines 43-50) or a burst mode of operation (col. 6 lines 14+); selection and temporary storage circuit (Fig. 1 Ref. 18) and a first external address (col. 4 lines 16-18 or lines 22-24) and a second external address (col. 5 lines 43-50); a counter (col. 8 lines 58+); and a pair of multiplexer (Fig. 1 Ref 40 and Fig. 5 Ref. 66, multiplexing input address, col. 4 line 19 and selection of external address or internal counter, col. 8 lines 58+).

Response to Amendment

7. Applicant's arguments filed on 5/4/01 have been fully considered but they are not persuasive.

Applicant's remarks on pages 4-6 concerning the references not teaching switching between a burst mode and pipeline mode is not considered persuasive.

Oki discloses a memory circuit comprises control logic (page 2 BE pin) and receiving an initial external address (page 2 A). Although Oki discloses control logic for burst and normal page, Oki does not specifically disclose a pipeline mode. However it was well known in the memory art at the time the invention was made to use the pipeline mode to access memory per each cycle thereby increasing the access speed. For example, Manning discloses limitation of "the current invention include a pipelined architecture" (col. 5 lines 43-49) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55), in other words, Manning discloses a mode circuitry to select between fast page pipeline and burst since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed. Therefore, broadly written claims are disclose by the references cited.

Also page 77 in "Rossini, Pentium, PCI-ISA, Chip set", Symphony Laboratories, June 1995 (See IDS filed on 3/2/1999) also discloses selecting between burst and burst pipeline in SRAM. Therefore, broadly written claims are disclose by the references cited.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

10. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

12. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

14. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-6296 or (703) 308-6165

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Patent Examiner
July 27, 2001